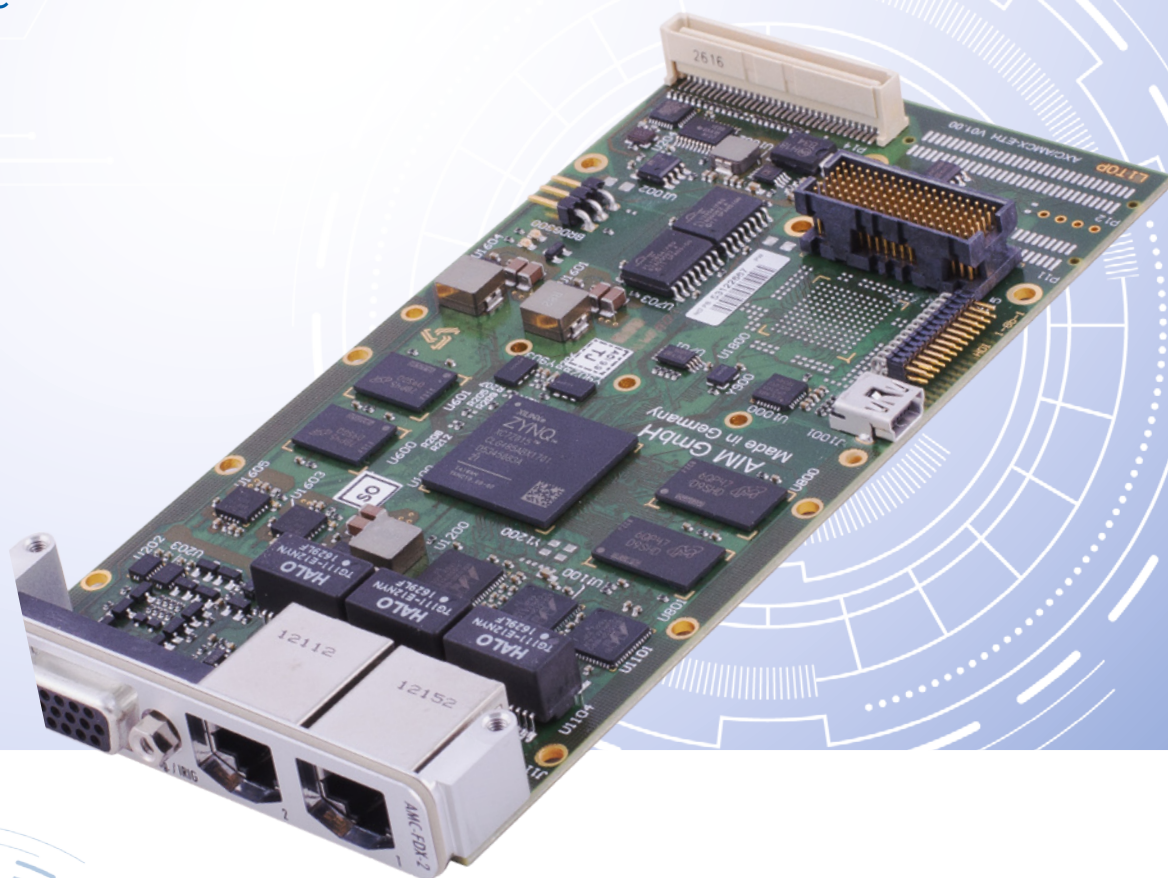


AXC-FDX-2

2 Port 10/100/1000Mbit/s
AFDX®/ARINC664P7
Test, Simulator and Monitor
Module for XMC

Data
Sheet



AXC-FDX-2

General Features

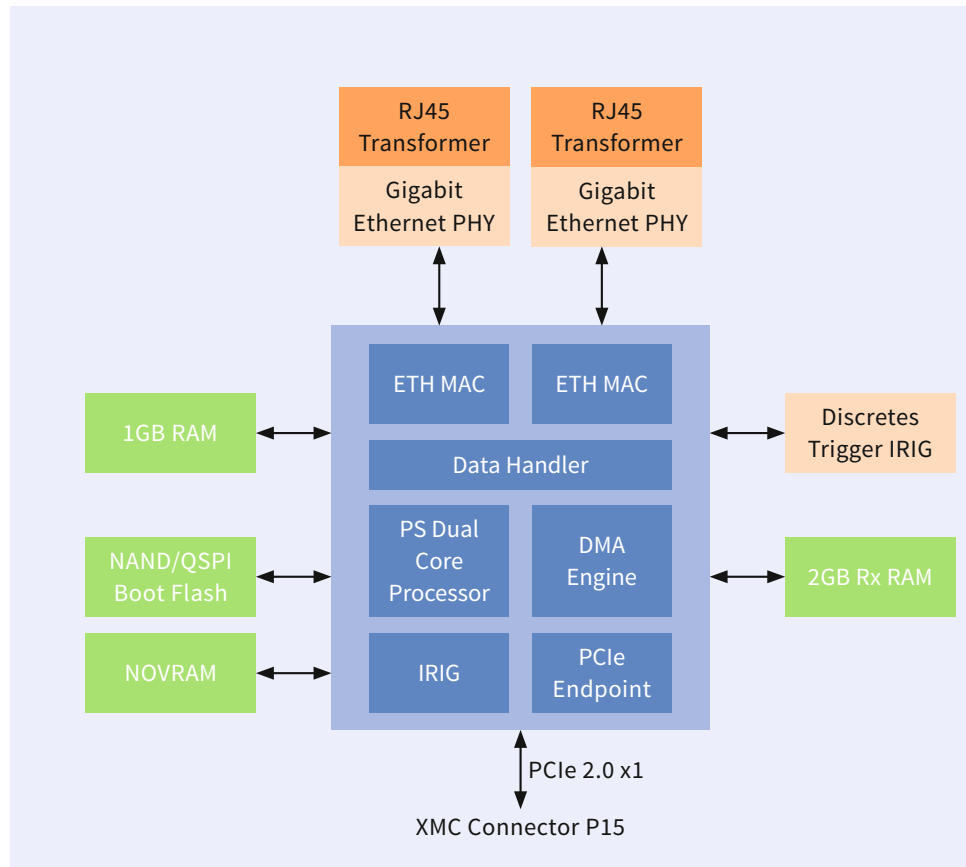
The ► **AXC-FDX-2** is AIM's new high performance XMC module offering full function test, simulation, monitoring and analyzer functions for ► **AFDX®/ARINC664P7** (Avionics Full Duplex Switched Ethernet) networks. Versions available for both Airbus and Boeing variants of the ARINC664P7.

The board supports the Boeing ARINC664 extensions for EDE at the hardware interface layer with field proven real time simulation of EDE subscribers to meet all parts and multiple revisions of the EDE specifications. Its unique onboard processing capability, memory resources, customized AFDX® MACs and IRIG-B time code decoder/generator gives AFDX® users a comprehensive feature set for the most demanding AFDX® applications.

The AXC-FDX-2 module provides two AFDX® ports being configured as two single or one dual redundant port each implementing a 10/100/1000Mbit/s full duplex Ethernet interface. Ports can operate concurrently in traffic simulator or receiver/monitor modes with support for AFDX® port related frame statistics. Virtual Link (VL) packet capturing and monitoring features are complimented with powerful triggering and filtering capabilities. An integrated TAP mode enables analyzing network traffic in-line, with all onboard and PBA.pro features between two attached Ethernet devices.

The extensive memory resources onboard allow to implement large receive buffers and complex transmit scenarios onboard. An AFDX®/ARINC664P7 specific Physical Bus Interface implements two full duplex ports for connection to AFDX® networks.

AXC-FDX-2 Block Diagram



The AXC-FDX-2 module is available with the optional ► **PBA.pro** analyzer software package for Windows and Linux.

- 10/100/1000Mbit/s Ethernet compliant Frontend
- Designed for Applications such as:
 - Test and Verification of End Systems
 - Switch Testing
 - Monitoring of Traffic between End Systems and Switch
 - Inter Switch Traffic Analysis
 - Multi Stream High Level System Integration
- Programmable Ports – Traffic Simulator and Receiver/Monitor Concurrently
- Synchronized Timing across Multiple Modules
- Driver Software for Windows and Linux

Traffic Generation

The AXC-FDX-2 provides real time traffic generation on both ports concurrently. Transmitter operation allows users to fully programme all fields of the AFDX®/ARINC664P7 frame including the Virtual Link

identifier, MAC source address, IP structure, UDP structure, payload and sequence number. Multiple modes of transmit sequencing are supported, these being generic/replay and UDP port oriented shaped transmissions. Users can program payload data with user defined or fixed data. Inserting the time tag in the payload data provides an elegant solution to measure frame transmit delays through the network. Synchronization of transmissions across multiple ports is achieved by using strobe inputs/outputs.

- Programmable Timing and Sequencing of Frames
- Physical Error Injection – CRC, Gap, Size, Alignment
- Logical Error Injection on Layers 2, 3, 4
- Timing Error Injection – Violation of Bandwidth Allocation Gap (BAG)
- Autonomous Dynamic Data Generation
- UDP Port Simulation with Traffic Shaping and Sequence Numbering
- Onboard Support for Sampling and Queuing Ports

UDP/VL Receive Mode

The ► **AXC-FDX-2** module ports can be configured to work in UDP/VL oriented receive mode. In this mode each UDP port has a separate buffer queue. Received frames are stored with frame headers containing time tag and status information. Frame header information can be stored and payload data optionally discarded for the testing of switches and the complete network. With the traffic shaping verification enabled, any violations are reported as errors in related frame headers.

- VL oriented Filtering
- Second Level Filtering on Generic Frame Parameter
- Time Stamping of Received Packets with extended IRIG-B Time Code
- Physical Error Detection, Frame Level – CRC, Gap, Size and Alignment
- AFDX® Specific Error Detection
- Traffic Shaping Verification
- Verification of MAC, IP and UDP Headers
- VL oriented Integrity Checking

Chronological Receive Mode (Monitor Mode)

The AXC-FDX-2 module ports can be configured in chronological receive mode to sequentially receive frames and store them in a circular buffer. The payload data can be discarded to optimize the use of the buffer for frame capture and analysis.

Powerful filtering, triggering, complex triggering and capture modes allows users to select only the frames, data and errors of interest. Monitor mode also provides activity monitoring and statistics for each VL recorded by the AXC-FDX-2 module. The interface modules report the number of frames received and the number of errors detected globally and in VL orientated format.

- VL orientated Receive and Filtering
- Second Level Filtering on Generic Frame Parameters
- Chronological Monitor with Time Stamping
- Massive onboard Monitor Buffer
- Inter Frame Gap Time Measurements with 8ns Resolution
- Comprehensive Triggering/Filtering/Capturing
- Programmable Data Capture Modes – Trace after Trigger and Recording
- Physical Error Detection – CRC, Gap, Size and Alignment
- AFDX®/ARINC664P7 specific Error Detection

TAP Mode

The AXC-FDX-2 can operate in TAP mode in all network speeds. This allows to analyze the network traffic between two attached network devices. Inter-message-timing will not be changed in this operational mode and network data will not be modified ensuring full operation of attached ports.

Time Synchronization

An onboard IRIG-B time code decoder and generator allows synchronization of multiple AFDX® ports using multiple AXC-FDX-2 modules. Modules can be synchronized using an external IRIG-B time source or the onboard time code generator of one module as the reference for accurate correlation of data across multiple AFDX®/ARINC664P7 ports.

Physical Bus Interface

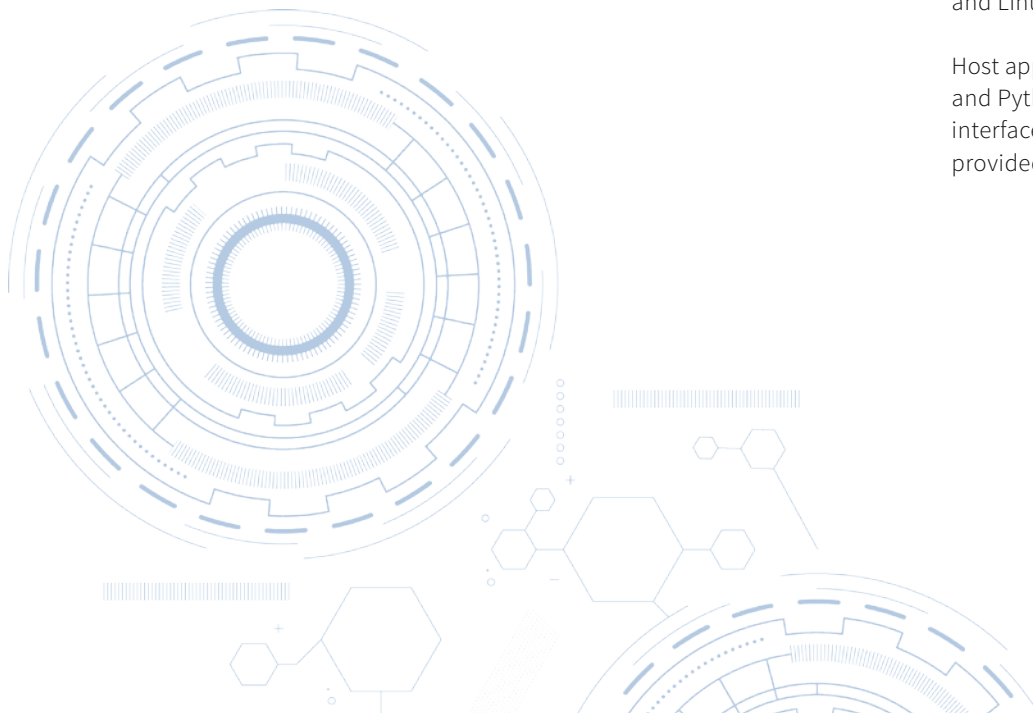
The AXC-FDX-2 modules provide two AFDX® ports which can be used as two single channels or as one dual redundant channel AFDX® specific physical bus interface.

- Customized Media Access Controllers (MAC's) implemented in FPGA (► **SoC**), optimized for AFDX®/ARINC664P7
- 3GByte DDR3 Memory for System, Receiver and Transmitter Buffer
- Physical Interface and Magnetics (COTS)
- 8-Socket Network Interface Connectors – RJ45
- Trigger, Strobe and Time Code I/O Connector

Driver Software Support

The driver software is supplied with the AXC-FDX-2 module. A full functional Application Programming Interface (API) is provided compatible with Windows and Linux.

Host applications can be written in C/C++ and Python. A LabView/VI application interface as well as LabViewRT drivers are provided.



Technical Data

System Interface

XMC/PCIe Single Lane, compliant to PCIe V2.0

Processors

Dual Core Processing System, integrated in SoC Device

Memory

1GByte DDR3 Processing System RAM

2GByte DDR3 MAC Receiver RAM

Encoder/Decoder

2 AFDX® specific Ethernet MAC's, integrated in SoC Device;

Inter Frame Gap Generation and Measurement with 8ns Resolution (1000Mbit/s Operation)

Time Tagging

46-bit absolute IRIG-B Time with 100ns Resolution;

Inter Frame Gap Generation and Measurement with 8ns Resolution

Physical Bus Interface (PBI)

2 full duplex AFDX® Ports configurable to

1 dual-redundant AFDX® Port or to

1 TAP Port

Connectors

2 x 8 way RJ45 Connectors, 1 per AFDX® Port; 1 x 15 way D-Sub Connector (female) for Time Code, Discrete I/O and Trigger I/O; XMC Connector P15 for Single Lane 5Gb/s PCI Express Bus

Dimensions

Single Width XMC Standard: 149mm x 74mm

Power Consumption

Typical 4.7W (10/100Mbit/s) /

5.5W (1000Mbit/s) (operating)

Operating Temp. Range

Standard: 0°C to +55°C ambient

Extended: -20°C to +75°C ambient on Request

Storage Temp. Range

-40°C to +85°C ambient

Humidity

0 to 95% non-condensing

Versions available for both Airbus and

Boeing variants of the ARINC664P7

* AFDX® is a registered trademark of Airbus

Ordering Information

AXC-FDX-2

2 Port, 10/100/1000Mbit/s

AFDX®/ARINC664P7 XMC Module: Traffic Simulator, Receiver and Chronological Monitor, Integrated Tap Mode, IRIG-B Time Decoder, 3GB DDR3 RAM Includes Driver Software for Windows, LabVIEW VI's, LabVIEW RT, Linux

AXC-FDX-2-G

2 Port, 10/100/1000Mbit/s

AFDX®/ARINC664P7 XMC Module: Generic TX/RX Function Only, Integrated Tap Mode, IRIG-B Time Decoder, 3GB DDR3 RAM

Includes Driver Software for Windows, LabVIEW VI's, LabVIEW RT, Linux

AXC-FDX-2B

2 Port, 10/100/1000Mbit/s

AFDX®/ARINC664P7 XMC Module: Traffic Simulator, Receiver and Chronological Monitor, Integrated Tap Mode, IRIG-B Time Decoder, 3GB DDR3 RAM Including Boeing EDE Specific Extensions Includes Driver Software for Windows, LabVIEW VI's, LabVIEW RT, Linux

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