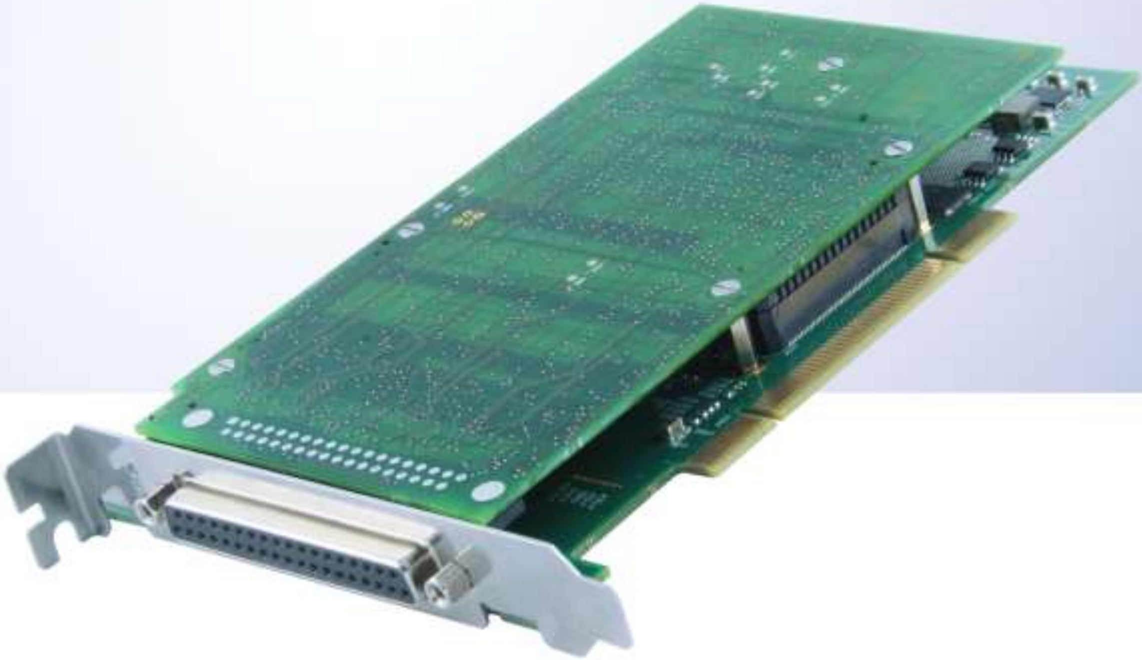
APXX429

4/8/16 Channel ARINC429
Test & Simulation Module
for PCI

Avionics Databus
Solutions



Hardware Manual

V01.02 Rev. B
January 2025

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DOCUMENT HISTORY

The following table defines the history of this document.

Version	Cover Date	Created by	Description
V01.00 Rev. A	18.04.2018	M. Lamp	First Released Version (Rename from APXE to APXX Change block figure, power consumption)
V01.00 Rev. B	08.05.2018	M. Lamp	Correct year on top sheet (was 2017)
V01.01 Rev. A	14.04.2022	M.Masood	Added chapter “Front Panel LEDs”
V01.02 Rev. A	20.12.2024	M. Maier	Chapter 4: trigger length corrected
V01.02 Rev. B	30.01.2025	M. Maier	Clarify trigger pulse length

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 INTRODUCTION

1.1 General

This document comprises the Hardware User's Manual for the PCI APXX429-4/8/16 which implements 4/8/16 transmit and 4/8/16 receive ARINC-429 channel, based on the PCI bus standard. The document covers the hardware installation, board connections, technical data and a general description of the hardware architecture. For programming information please refer to the documents listed in the 'Applicable Documents' section.

Following Table describes the ARINC channel availability of the different APXX429 Modules:

Product Name	No. of Transmit Channels controllable Ampl.	No. of Transmit Channels fixed Ampl.	No. of RX Channels	Interface Mode
APXX429-4	4	---	4	Separate Rx/Tx-Pins
APXX429-8	8	---	8	Separate Rx/Tx-Pins
APXX429-16	8	8	16	Shared Rx/Tx-Pins

Table 1: channel availability of different APXX429 modules

The APXX429 module is a member of AIM's new family of advanced PCI modules compatible to PCI Standard (Release 3.0) 32 bits.

On the transmit channels, the APXX429 acts as an autonomously operating bus traffic simulator, supporting multiple modes of transmission sequencing. Full error injection capabilities are available, whereby the error injection is programmable individually for each channel and label. For special transmission operating modes the parity bit can be used alternatively as an additional data bit. The rise and fall time of the bus signals are individually programmable by software for each transmit channel.

For the receive channels, the APXX429 provides an advanced monitor and analyser function with unique on-board error detection, triggering and filtering capabilities. Monitor and analyser functions are available concurrently and independent from each other. The hardware architecture provides resources to guarantee that the performance of one function is not affected by the current load of the other function. The rise and fall times of the bus signals are individually programmable for each receive channel. To adapt to different transmit speeds; the transmission rate can be varied in discrete steps between approximately 90 and 120kBits on the high speed bus and between 11.5 and 16.0kBits on the low speed lines. The discrete steps are global for all channels.

The hardware architecture provides ample resources (i.e. processing capability and memory) to guarantee, that all specified interface functions are available concurrently and to full performance specifications.

The advanced architecture uses a special processor for the ARINC-429 streams. A powerful PCI-Express Controller and Memory Arbiter is implemented in a Field Programmable Gate Array (FPGA). The connection to the PCI Bus is done via a PCIe to PCI bridge device. This FPGA supports both, the interface to the application and driver software tasks running on the host computer and assists the communication for data transfer. This feature expands the capability of the APXX429 module to that of a high level instrument. To fulfil the real-time requirements of a typical avionic type data bus system, a high performance 32bit RISC processor (BIP) is implemented.

A free wheeling IRIG-B Time code Encoder/Decoder is implemented on the APXX429 to satisfy the requirements of 'multi-channel time tag synchronization' on the system level. The IRIG-B compatible amplitude modulated sine wave output allows the synchronization of any external module implementing IRIG-B time stamping.

1.2 How This Manual Is Organized

This APXX429 Hardware Manual is comprised of the following sections.

Section 1 - Introduction - contains an overview of this manual.

Section 2 - Installation - describes the steps required to install the APXX429 device and connect the device to other external 429 interfaces, IRIG-B, and triggers.

Section 3 - Structure of the APXX429 - describes the physical hardware interfaces on the APXX429 using a block diagram and a description of each main component

Section 4 - Technical Data - describes the technical specification of the APXX429.

1.3 Applicable Documents

The following documents shall be considered to be a part of this document to the extent that they are referenced herein. In the event of conflict between the documents referenced and the contents of this document, the contents of this document shall have precedence.

1.3.1 Industry Documents

PCI Express BUS Specification; PCI-SIG Revision 1.1
PCI BUS Specification; Release 3.0; 32 bits

1.3.2 Product Specific Documents

AIM - Reference Manual APXX429 Application Interface Library
Detailed description of the programming interface between the Host Carrier board and the on-board driver software.

2 INSTALLATION

2.1 Preparation and Precaution for Installation

The APXX429 features full PCI Plug and Play capability; therefore, there are no jumpers or switches on the board that require modification by the user in order to interface to the PCI bus.

It is recommended to use a wrist strap for any installations. If there is no wrist wrap available, then touch a metal plate on your system to ground yourself and discharge any static electricity during the installation work.

2.2 Installation Instructions

The following instructions describe how to install the APXX429 module in your system. Please follow the instructions carefully, to avoid any damage on the device.

▶ **To Install the APXX429**

1. Shutdown your system and all peripheral devices.
2. Unplug the power cord from the wall outlet. (Inserting or removing modules with power applied may result in damage to module devices).
3. Remove the system cover to gain access to the system slots.
4. Find a free PCI slot in your system
5. Remove the slot bracket from the slot you have chosen and put the screw aside.
6. Align the APXX429 card slot connector with the PCI slot and gently lower the card into the free slot.
7. Secure the card to the PCIe slot with the screw you removed from the metal plate. Ensure the module is seated properly in the slot connector.
8. Replace the cover of your system.
9. Connect the system to the power source. Turn on the power to your system.

2.3 Connecting to Other Devices

The connection to other devices is done via a DSUB-37 female connector. Due to the product variety of the APXX429 modules, the pinout of the DSUB37 connector is dedicated to each single product type.
At some product types, the ARINC429 Receive/Transmit channels are either share the pins on the front panel connector or Receive and Transmit signals are located on different pins. If the Receive signals and the Transmit signals of one ARINC429 channel are assigned to different pins on the DSUB37 connector, then the module is configured in 'Downward Compatibility' Mode, which means that the module implements the identical pinout than the corresponding APXX429 module. Otherwise, the APXX429 implements the capability to share the I/O- pins of one ARINC429 channel between the Transmit and the Receive functionality, but only either operation mode at the same time.
The pinouts for the different APXX429 products is listed below:

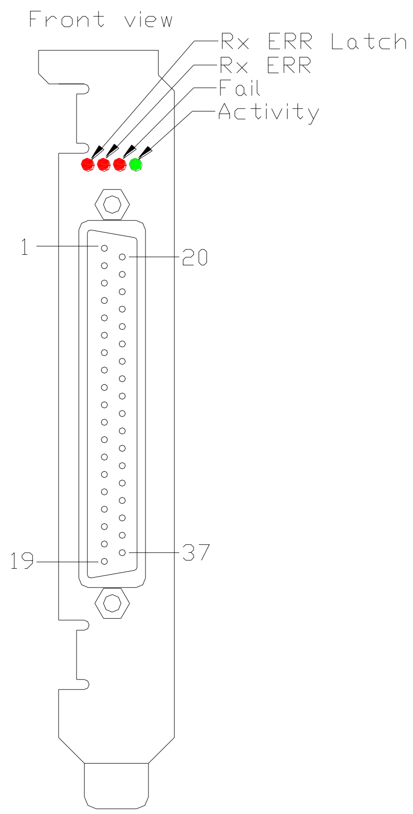


Figure 2-1 Front plate view

2.3.1 APXX429-4 Front Panel Connector Pinout

37 pin D-SUB female connector, Downward Compatibility Mode

Pin	Signal Description	Pin	Signal Description
1	Tx Channel 1 (True)	20	Tx Channel 1 (Complement)
2	Tx Channel 2 (True)	21	Tx Channel 2 (Complement)
3	Tx Channel 3 (True)	22	Tx Channel 3 (Complement)
4	Tx Channel 4 (True)	23	Tx Channel 4 (Complement)
5	Reserved	24	Reserved
6	Reserved	25	Reserved
7	Reserved	26	Reserved
8	Reserved	27	Reserved
9	Trigger In 0	28	IRIG Out
10	Ground		Reserved
11	Trigger Out 0	29	IRIG In
12	Rx Channel 1 (True)	30	Rx Channel 1 (Complement)
13	Rx Channel 2 (True)	31	Rx Channel 2 (Complement)
14	Rx Channel 3 (True)	32	Rx Channel 3 (Complement)
15	Rx Channel 4 (True)	33	Rx Channel 4 (Complement)
16	Reserved	34	Reserved
17	Reserved	35	Reserved
18	Reserved	36	Reserved
19	Reserved	37	Reserved

Table 2: Pin assignment APXX429-4

2.3.2 APXX429-8 Front Panel Connector Pinout

37 pin D-SUB female connector, Downward Compatibility Mode

Pin	Signal Description	Pin	Signal Description
1	Tx Channel 1 (True)	20	Tx Channel 1 (Complement)
2	Tx Channel 2 (True)	21	Tx Channel 2 (Complement)
3	Tx Channel 3 (True)	22	Tx Channel 3 (Complement)
4	Tx Channel 4 (True)	23	Tx Channel 4 (Complement)
5	Tx Channel 5 (True)	24	Tx Channel 5 (Complement)
6	Tx Channel 6 (True)	25	Tx Channel 6 (Complement)
7	Tx Channel 7 (True)	26	Tx Channel 7 (Complement)
8	Tx Channel 8 (True)	27	Tx Channel 8 (Complement)
9	Trigger In 0	28	IRIG Out
10	Ground		
11	Trigger Out 0	29	IRIG In
12	Rx Channel 1 (True)	30	Rx Channel 1 (Complement)
13	Rx Channel 2 (True)	31	Rx Channel 2 (Complement)
14	Rx Channel 3 (True)	32	Rx Channel 3 (Complement)
15	Rx Channel 4 (True)	33	Rx Channel 4 (Complement)
16	Rx Channel 5 (True)	34	Rx Channel 5 (Complement)
17	Rx Channel 6 (True)	35	Rx Channel 6 (Complement)
18	Rx Channel 7 (True)	36	Rx Channel 7 (Complement)
19	Rx Channel 8 (True)	37	Rx Channel 8 (Complement)

Table 3: Pin assignment APXX429-8

2.3.3 APXX429-16 Front Panel Connector Pinout

37 pin D-SUB female connector Shared Pin Mode

Pin	Signal Description	Pin	Signal Description
1	Tx/Rx Channel 1 (True)	20	Tx/Rx Channel 1 (Complement)
2	Tx/Rx Channel 2 (True)	21	Tx/Rx Channel 2 (Complement)
3	Tx/Rx Channel 3 (True)	22	Tx/Rx Channel 3 (Complement)
4	Tx/Rx Channel 4 (True)	23	Tx/Rx Channel 4 (Complement)
5	Tx/Rx Channel 5 (True)	24	Tx/Rx Channel 5 (Complement)
6	Tx/Rx Channel 6 (True)	25	Tx/Rx Channel 6 (Complement)
7	Tx/Rx Channel 7 (True)	26	Tx/Rx Channel 7 (Complement)
8	Tx/Rx Channel 8 (True)	27	Tx/Rx Channel 8 (Complement)
9	Trigger In 0	28	IRIG Out
10	Ground		
11	Trigger Out 0	29	IRIG In
12	Tx/Rx Channel 9 (True)	30	Tx/Rx Channel 9 (Complement)
13	Tx/Rx Channel 10 (True)	31	Tx/Rx Channel 10 (Complement)
14	Tx/Rx Channel 11 (True)	32	Tx/Rx Channel 11 (Complement)
15	Tx/Rx Channel 12 (True)	33	Tx/Rx Channel 12 (Complement)
16	Tx/Rx Channel 13 (True)	34	Tx/Rx Channel 13 (Complement)
17	Tx/Rx Channel 14 (True)	35	Tx/Rx Channel 14 (Complement)
18	Tx/Rx Channel 15 (True)	36	Tx/Rx Channel 15 (Complement)
19	Tx/Rx Channel 16 (True)	37	Tx/Rx Channel 16 (Complement)

Table 4: Pin assignment APXX429-16

2.4 Front Panel LEDs

Four sub miniature LED's, as listed in Table 5, indicate the various conditions of the module at the front panel. The LED's are located in a quadruple LED- Array on the physical interface daughterboard. The first LED is used for indication of ARINC429 data streams of one or more channels. If data are transmitted, the green LED will be flashed. The second LED is used for board fail indication. If the board or any of the self-test routines have failed, the red LED will still be illuminated after power-up. After power-up, this LED is illuminated for app. 5 seconds. The third and fourth LED is used for error indication in a received data stream on any of the sixteen (eight) channels. If any error occurs, the third red LED will be flashed. The error event is stored and leads to an illumination of the fourth LED. During power-up or reset all LEDs are illuminated for self-test purposes.

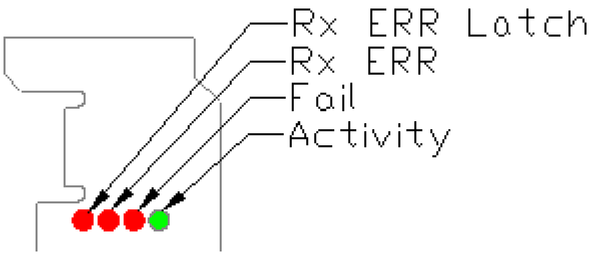


Figure 2-2: Status LED view

LED Name	Colour	Description
ACTIVITY	Green	LED flashes If data is transmitted on any channel.
FAIL	Red	LED illuminates if an error during the BIU self-test occurs.
RX-ERR	Red	LED flashes if an error on any channel is detected.
RX-ERR-LATCH	Red	LED illuminates if an error on any channel is detected (stored error).

Table 5: Front Panel LED description

3 STRUCTURE OF THE APXX429

The structure of the APXX429 board is shown in [Figure 3-1]. The APXX429 comprises the following main sections:

- PCI-Express bus and BIU-IO FPGA
- PCI-Express to PCI bridge
- Global RAM
- BIU Processor Section
- Physical I/O Interface with 4/8/16 ARINC-429 Channel, Trigger and Discretes
- IRIG- Time Code Processor with Free Wheeling Function and Sine Wave Output
- Boot-Up Flash

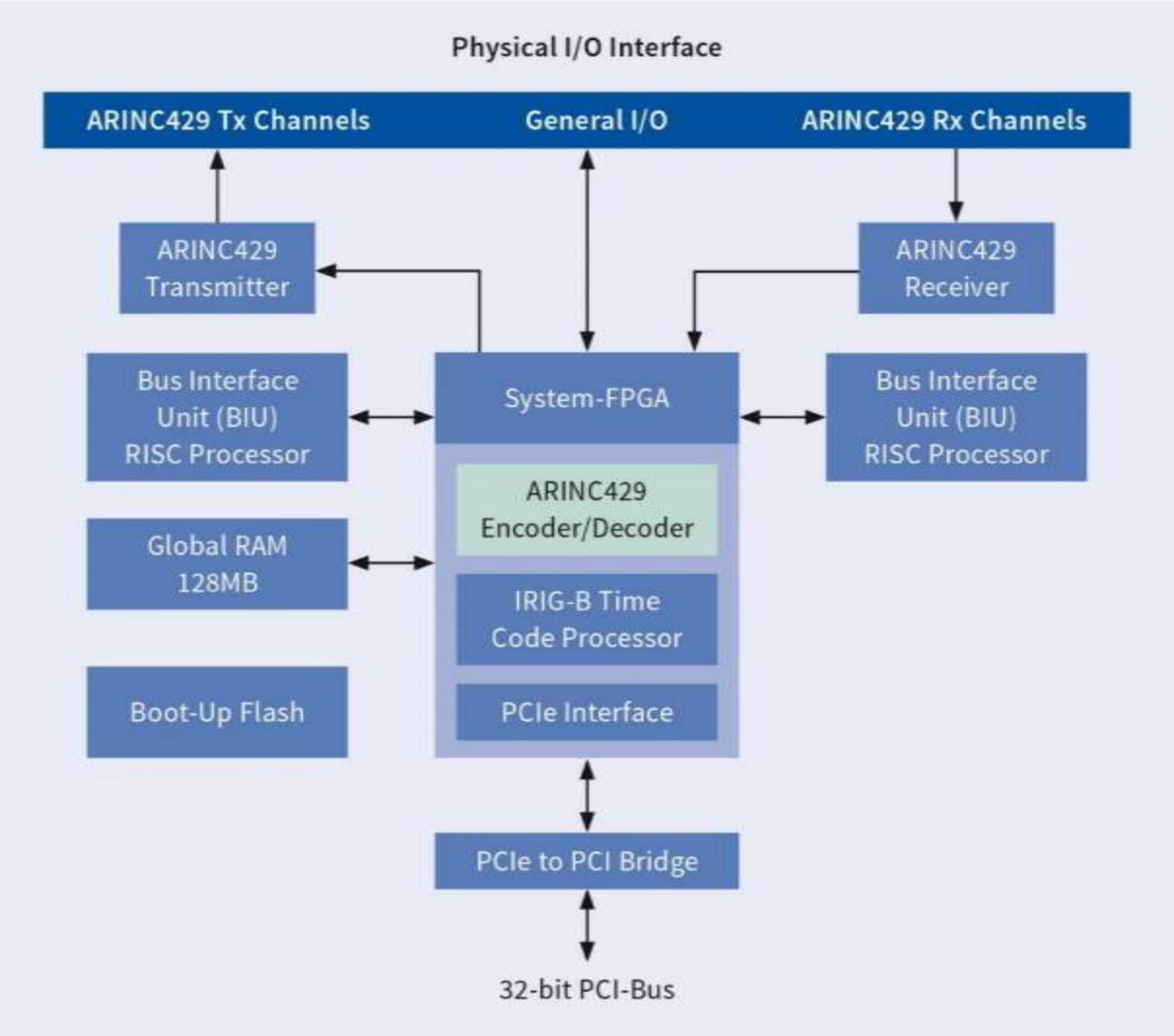


Figure 3-1: Block Diagram of APXX429

3.1 PCI-Express bus and BIU-I/O FPGA

The new common FPGA architecture of AIM's PCI-Express family includes both the complete PCI-Express bus logic and the BIU processor logic. This programmable device implements the following features:

- PCI Express 1.1 compliant bus interface
- Global RAM interface and arbitration
- Boot function
- SPI controller for update programming
- ARINC-429 Encoder
- ARINC-429 Decoder
- IRIG Encoder and decoder support
- External Trigger Inputs and Outputs
- Up to eight user definable Discrete I/Os

3.2 PCI-Express to PCI Bridge

The transparent bridge connect the PCI Bus (32Bit, 66MHz) to the local Card intern PCIe Bus.
For power mangment and configuration a Flash device is available.

3.3 Global RAM Interface and Arbitration

The common FPGA implements a Global RAM arbiter, which controls the Global RAM access between both participants, the Host through the PCI-Express bus and the BIU processor.

3.4 Boot up

To provide maximum flexibility and upgradeability, the FPGA device and the processors are booted automatically from dedicated SPI-Flashes after power up.

3.5 Global RAM

The Global RAM is shared between both BIU processors (BIP) and the Host-Card Bus. The arbitration is handled by the common FPGA. It has access to the common Global RAM via a 32 bit wide data port.

3.6 BIU-Processor (BIP)

There are two physical BIU processors. Each BIP consists of an ultra-low power, high performance 32bit RISC processor.

3.7 ARINC-429 Encoder

The encoder converts the parallel data into a serial ARINC429 encoded data stream and appends the parity and the gap bits. The programmable frame times between two labels can be set in the range from 0 up to 255 ARINC429 bits.

The encoder provides the following error injection capabilities:

- Gap Error (-1 bit)
- Bitcount Error (+/- 1 bit)
- Coding Error (fixed at bit position 12)
- Parity Error (if no special transmission mode is chosen)

3.8 ARINC-429 Decoder

The decoder converts the serial received data stream into a parallel data double word and generates an additional 16 bit report for each received label. The decoder measures the gap time between two labels for gap error detection and bus load traffic detection.

The decoder provides the following error detection capabilities:

- Gap Error Detection
- Bit count Error Detection
- Coding Error Detection
- Parity Error Detection (if no special transmission mode is chosen)

3.9 External Trigger Inputs and Outputs

One Trigger input and one Trigger output is provided for all APXX429 variants

The Trigger I/Os are TTL level compatible. Filter circuitry is provided at the trigger inputs and outputs to cover Electromagnetic Compatibility (EMC) aspects.

The Trigger output pulse has a minimum length of 500ns.

3.10 IRIG- and Time Code Section

The main functions of the Time Code Processor (TCP) are:

- IRIG-B compatible Time Code Decoder function
- Time code Encoder – IRIG-B compatible Time Encoder function

3.10.1 Time Code Encoder/Decoder

The generated time code signal is an IRIG-B compatible sinusoidal waveform. The time code information can be used for time-tagging and multi-channel synchronization. On the APXX429 a new generation IRIG-B section is implemented with a free wheeling IRIG functionality. If no external IRIG signal is detected, the TCP switches automatically to the free wheeling mode. Also, if an external IRIG-B signal is detected in free wheeling mode, the Time tag is automatically synchronized to this external IRIG-B signal.

The time tag on the board is generated in the following format in Table 6.

Time Element	Number of bits
DAYS of Year	9
HOURS of Day	5
MINUTES of Hour	6
SECONDS of Minute	6
MICROSECONDS of Second	20
Summary	46 (6 Bytes, stored in two 32bit words)

Table 6: IRIG-B: Binary Coded Time Tag

3.10.2 Time Tag Methods

The IRIG-IN and IRIG-OUT signals shall be connected depending on the time tag method used as shown below.

1. Single AIM-Module No External IRIG-B Source
No connection required

2. Multiple AIM-Modules with No Common Synchronization Requirement
No connection required

3. Single or Multiple AIM-Module(s) with External IRIG-B Source
Connect external IRIG-B source to IRIG-IN and GND of all modules

4. Multiple AIM-Modules with No External IRIG-B Source Internally Synchronized.
Connect the IRIG-OUT signal and the GND of the module you have chosen as the time master to all IRIG-IN signals (including the time master).

3.10.3 Board to Board(B2B) connector as IRIG In/Out

Normally for connecting the IRIG Input and/or Output the 37-pin DSUB is used for wiring. Follow the instructions below if the B2B connector is used instead.

The IRIG-B output signal can be manually switched to the B2B connector by setting the jumper position to “Master-Mode”.
To avoid signal collision only one board should drive the IRIG output signal.

The figure 3 below shows the on-board Board IRIG Master/Slave jumper (J0504) on the APXX429:

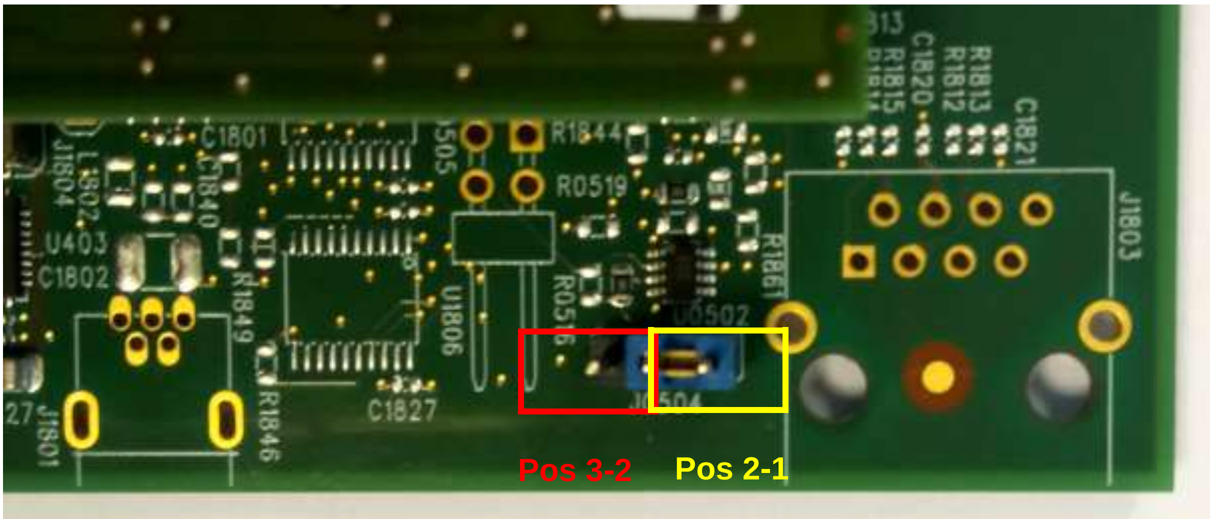


Figure 3-2: IRIG Jumper

If the board receives the IRIG signal, it is in IRIG Slave-Mode, if the board transmits the IRIG signal, it is in IRIG Master-Mode.

To set a board to IRIG Master-Mode (IRIG output), the jumper has to be set to position 1 and position 2.

To set a board to IRIG Slave-Mode (IRIG Input), the jumper has to be set to position 2 and position 3 or it can be removed (no jumper installed).

The on board generated IRIG output signal is available simultaneously on the B2B connector (if set to IRIG Master-Mode) and on the 429 Physical Bus Interface board (429 PBI).

To receive an external IRIG signal either the PBI IRIG input or the B2B connector IRIG input (IRIG Slave Mode) can be used (exclusive).

3.11 Board to Board Connector (B2B connector)

The Board to Board connector provides the eight GPIO Discrete I/O signals and an additional one pin combined IRIG-B Master-Output/Slave Input on a 16-pin ribbon cable connector (mounted on the upper right corner of the Board)

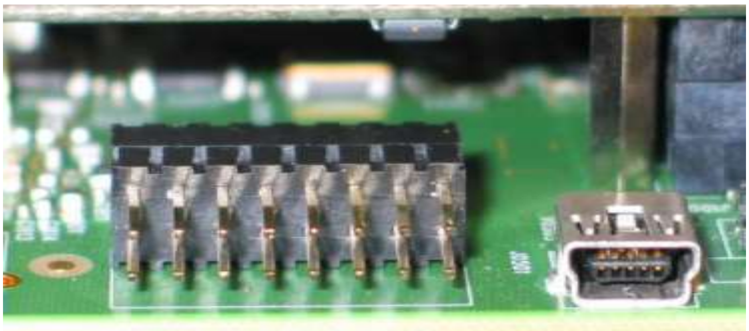


Figure 3-3: 16-Pin Ribbon-Cable-Connector

The connector provides the following signals:

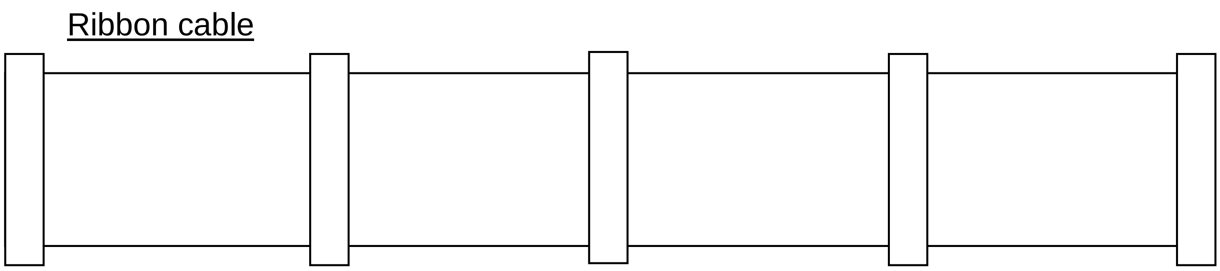
Pin	Signal Name	Comments
1	Reserved	Do not connect
2	Reserved	Do not connect
3	ASL GPIO 1	GPIO 1
4	ASL GPIO 2	GPIO 2
5	ASL GPIO 3	GPIO 3
6	ASL GPIO 4	GPIO 4
7	ASL GPIO 5	GPIO 5
8	ASL GPIO 6	GPIO 6
9	ASL GPIO 7	GPIO 7
10	ASL GPIO 8	GPIO 8
11	Reserved	Do not connect
12	IRIG	Master-Output / Slave-Input (select via J1702)
13	GND	
14	Reserved	Do not connect
15	Reserved	Do not connect
16	Reserved	Do not connect

Table 7: Pin-Out B2B Connector

For a detailed description how to select between IRIG Master and Slave operation see figure: "Figure 3-2: IRIG Jumper".

For connecting multiple APXX429 boards together a 16-pin standard ribbon cable with coded ribbon cable connector is used. It's important to use coded connectors to avoid damages caused by signal collisions.

The figure below shows a ribbon cable which could be used for connecting up to five APXX429 boards:



The figure below shows how the APXX429 boards can be connected together:

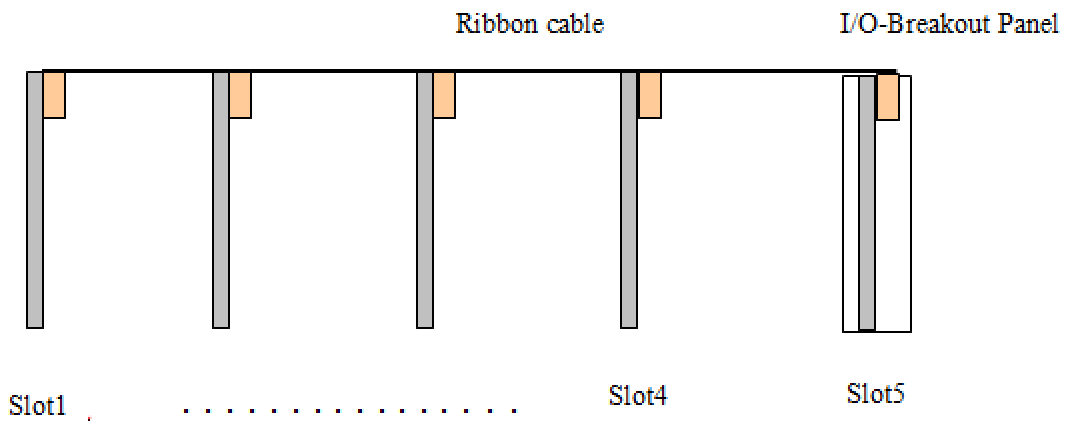


Figure 3-4: Ribbon Cable / Cable connection

If there is a requirement to provide the B2B connector signals externally (outside the PC), an optional AIM Breakout-Panel, which occupies one PC-Slot, can be used to get out the signals. Please ask for a Breakout Panel if there is a request.

The ribbon cable should not be directly connected (used) externally because the signals are not protected against over voltage.

3.12 General Purpose Discrete Inputs/Outputs (GPIO)

The APXX429 module provides eight user definable discrete I/O (GPIO's, which are available on the board to board connector) signals. Discrete input signals are always active whereas the discrete output signals are per default inactive. An open collector circuitry is used for the discrete output with approximately 4V provided by default. An external voltage from 0 to 35V can be supplied externally for switching higher voltages.

If the GPIO's should be provided external to the PC, a Breakout-Panel should be used.

NOTE:
The discrete outputs don't provide a series resistor for over current protection. In case a discrete input is used, make sure that the output-mode for that discrete is disabled, before connecting an external voltage, otherwise a high short circuit current to GND can damage the output transistor.

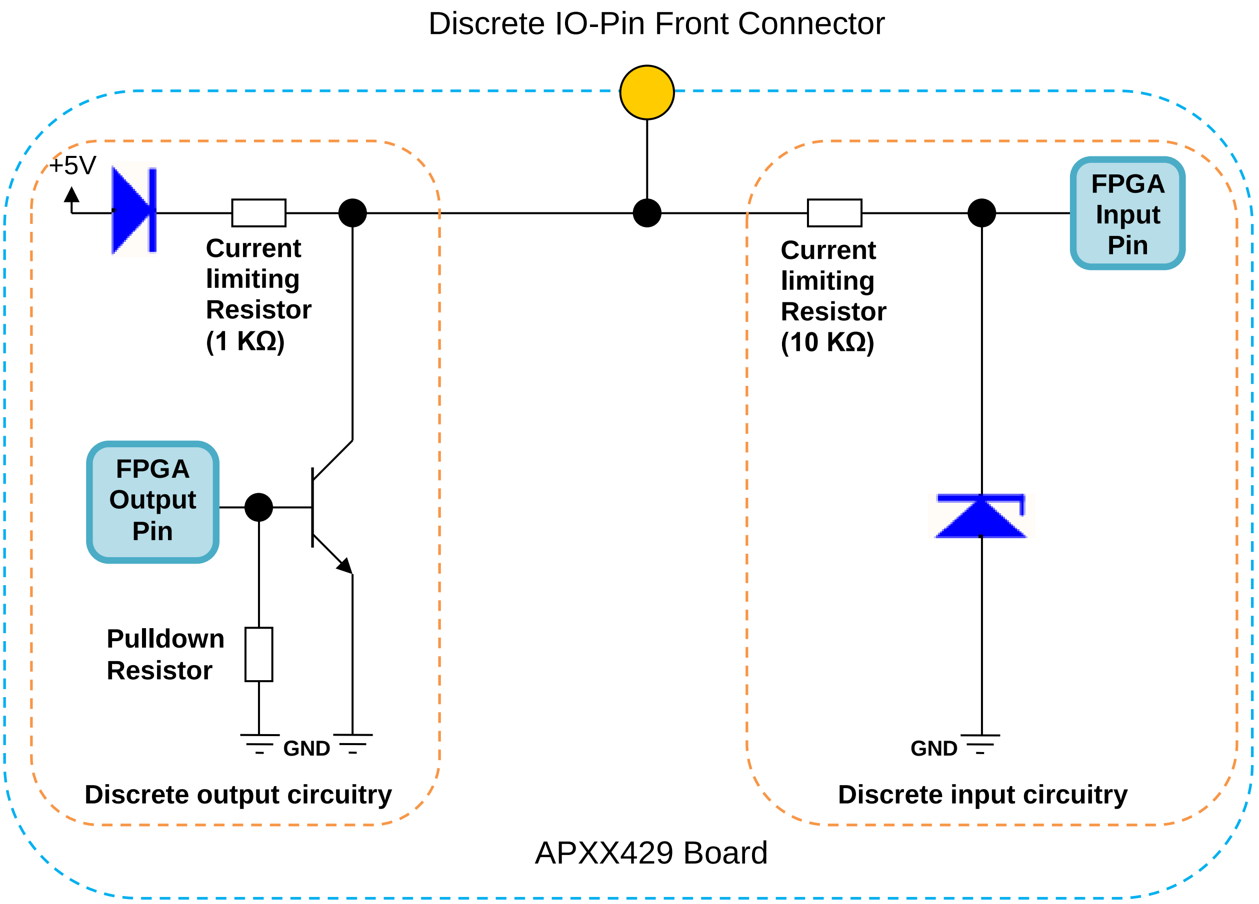


Figure 3-5: GPIO APXX circuitry

Be aware that a series resistor must be provided when a user voltage is used (Figure 3-6). This serial resistor must limit the current through the open collector transistor to max. current (see technical data chapter for details). Otherwise the open collector transistor can be damaged. EMC aspects are covered by filter circuitry.

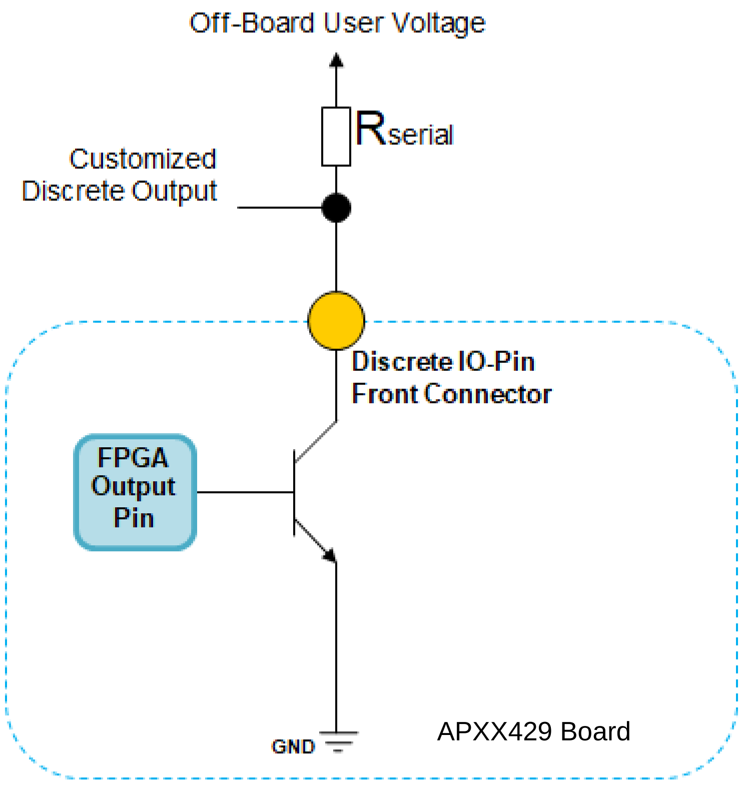


Figure 3-6: GPIO Protection with external resistor

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4 TECHNICAL DATA

PCI:

Compatible with PCI Standard Release 3.0 (32Bit, 33/66MHz) Universal add-in card with 5V tolerant I/Os, which plugs into both 3.3V and 5V connectors.

Memory:

- Fast Industrial DDR2-RAM, 128 MByte memory size, shared between BIU processor and PCI Express bus
- 128MBit SPI-Flash for FPGA
- 1kBit Serial SPI Flash for the PCI to >PCIe bridge

BIU-Section:

Low power, high performance 32bit RISC Processor(s); core speed 400 MHz

ARINC 429:

Line Transmitter:

Transmitter channel Output Impedance 75Ω
Channel 1-8 with variable output amplitude from 0 to ± 11V
Channel 9-16 with fixed output amplitude of typically ± 10V
High / Low Speed: Rise and Fall time automatically switched via Analogue Switches to meet the requirement for High / Low Speed operation

Line Receiver:

Input Impedance A to B: typ. 50kΩ
Input Impedance A/B to GND typ. 25kΩ

Encoder:

Programmable Bitrate High / Low Speed (100 / 12.5 Kbit/sec)
Programmable gap between two labels in the range from 0 up to 255 ARINC 429 bits.
ARINC429-Label Bit-32 programmable as Parity or additional Data Bit
Error injection capabilities:

- Gap Error (-1 bit)
- Bitcount Error (+/- 1 bit)
- Coding Error (fixed at bit position 12)
- Parity Error (if no special transmission mode is chosen)

Decoder:

Valid Receive Range Transmission speed select +/- appr. 10%
ARINC429-Label Bit-32 programmable as Parity or additional Data Bit
Measurement of gap between two labels in the range from 0.0 to 58.75Bits with 0.25Bit resolution.
Error detection capabilities:

- Gap Error Detection
- Bitcount Error Detection
- Coding Error Detection
- Parity Error Detection
  (if no special transmission mode is chosen)

Time Tagging:

IRIG B Time Tag:	For absolute time tagging, a special time code processor implements an IRIG-B encoder/decoder. If no external IRIG-B source is available a time code in IRIG B format is generated and can be used to synchronize multiple boards or modules.
Decoder:	- Format: IRIG-B-122 - Resolution: 1µs - Width: 1 Year (46 bits) - Signal Waveform: Amplitude modulated sine or square wave - Modulation Ratio: 3:1 to 6:1 - Input Amplitude: $0.5V_{pp}$ to $5V_{pp}$ - Input Impedance: > 10k ohm - Coupling: AC coupled - Time Jitter: +/- 5µs (depending on the input signal quality) - Lock time: < 5s Free wheeling accuracy after 10 Minutes < 1ppm (assuming input signal accuracy better than 50ppm)
Encoder:	- Format: IRIG B-122 - Absolute Accuracy: +/-25ppm (standard Oscillator) - Signal Waveform: Amplitude modulated sine wave - Output Amplitude: ~$4.5V_{pp}$, High voltage level - Modulation Ratio: ~3.2 : 1 - Carrier Frequency: 1kHz +/-50ppm

Connectors:

Front Connector:	37pol. Standard female DSUB
Board to Board Connector	Located on the Mainboard A 16-pin coded ribbon cable connector for the GPIO's and the system internal IRIG-B connection.

Trigger:

Trigger In:	TTL compatible Input Level, 10kΩ Pull Up resistor and high speed EMV varistor. Rising Edge sensitive, Pulsewidth > 75ns
Trigger Out:	Output with TTL Level; with high speed EMV varistor, High Pulsewidth strobe, minimum 500ns duration.

Discrete IO:

Eight user programmable, Input/Output selection done via software

Input High voltage	3.0V min	35.0V max
Input Low voltage	0.0V min	0.8V max

Output High voltage minimum 4V default, external voltage up to 35V max

Output Low voltage 0.4V max

Maximum Sink Current of each low active open collector 50 mA

NOTE: When the default 5V for the discrete outputs is not used, provide a serial resistor in line with the open collector transistor. If using a discrete pin as input, make sure that the output mode is set to inactive state before connecting an external voltage. Otherwise the transistor can be damaged. (Chapter 3.12).

The General Purpose Inputs and Outputs shall only be used for a Board to Board connection between multiple APX boards inside the PC.

If used for external connection, a AIM standard Breakout Panel should be used to get the GPIO's out of the PC and avoid board damage.

The AIM- Break Out Panel implements level shifter for the input signals as well as open collector outputs to drive aircraft compatible discrete IOs.

Supply Voltage: Standard PC – Supply +3.3V, +5.0V, +12.0V

Power Consumption	APXX429-4	APXX429-8	APXX429-16
IDLE:	3,3W	3,5W	4,3W
Operating HS [(1)]	3,3W	3,5W	4,6W
Operating LS [(2)]	3,3W	3,5W	4,5W
Operating LS [(3)]	4,5W	5,3W	7,6W

[(1)] High Speed 100 kHz; no load; 100 % Duty Cycle
[(2)] Low Speed 12,5 kHz; no load; 100 % Duty Cycle
[(3)] Low Speed 12,5 kHz; worst case load (400 Ohm || 30 nF); 100 % Duty Cycle

Dimensions: 107 x 168mm

Temperature:

0	to	+45°C	Standard Operating
-15	to	+60°C	Extended Temperature on request
-40	to	+85°C	Storage Temperature.

Weight: ~200g

Humidity: 0% to 95% non-condensing

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5 CERTIFICATE OF VOLATILITY

Model: APXX429

Part-Number: 121Cx-0101

Manufacturer: AIM GmbH
Sasbacher Str. 2
D-79111 Freiburg
Germany

Volatile Memory				
Does the item contain volatile memory (i.e., memory whose contents are lost when power is removed)? ☒ Yes ☐ No				
Description of used volatile memory:				
Type: DDR2-RAM	Size: 128 MByte	User Modifiable: ☒ Yes ☐ No	Function: Buffers, Descriptors, Global RAM	Process to Sanitize: Power off / on (Power Cycle)
Non-Volatile Memory				
Does the item contain non-volatile memory (i.e., memory whose contents are retained when power is removed)? ☒ Yes ☐ No				
Description of used non-volatile memory:				
Type: Serial SPI-Flash	Size: 64MBit	User Modifiable: ☐ Yes ☒ No	Function: FPGA Boot	Process to Sanitize: Erase
Type: Serial SPI-Flash	Size: 8MBit	User Modifiable: ☐ Yes ☒ No	Function: BIU1, Processor Boot	Process to Sanitize: Erase
Type: Serial SPI-Flash	Size: 8MBit	User Modifiable: ☐ Yes ☒ No	Function: BIU 2, Processor Boot	Process to Sanitize: Erase
Type: Serial SPI-Flash	Size: 1kBit	User Modifiable: ☐ Yes ☒ No	Function: Bridge Configuration	Process to Sanitize: Erase
Media				
Does the item contain media storage capability (i.e., removable or non-removable disk drives, tape drives, memory cards, etc.)? ☐ Yes ☒ No				
Description of used media storage:				
Type: -None-	Size: -	User Modifiable: ☐ Yes ☐ No	Function: -	Process to Sanitize: -
Additional Information:				
Test Engineer				
Name: Matthias Lamp	Title:		Date of Certification: 13.02.2018	

All operating Data for handling the I/O Protocol will be stored in volatile memory only. No Transfer data is stored in Non-Volatile Memory. The Non-Volatile Memory only contains production relevant data for board personalisation, FPGA Logic or Firmware Code for the on board Microcontroller.

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6 NOTES

6.1 Acronyms

ARINC	AERONAUTICAL RADIO, INC.
ADC	Analog to Digital Converter.
ARM	Advanced RISC Machine
BIP	Bus Interface Processor.
BIU	Bus Interface Unit.
BSP	Board Software Package
EMC	Electromagnetic Compatibility
FLASH	Page oriented electrical erasable and programmable memory.
FPGA	Field programmable Gate Array
GND	Ground
IRIG B	Inter Range Instrumentations Group Time code Format Type B
I/O	Input / Output
JTAG	Joint Test Action Group (IEEE 1149.1 Boundary Scan)
LCA	XILINX Logic Cell Array (Field Programmable Logic)
ns	nanosecond
PC	Personal Computer
PCB	Printed Circuit board
PCI	Peripheral component interconnect
PROM	Programmable Read Only Memory
RISC	Reduced Instruction Set Computer
RAM	Random Access Memory
SDRAM	Synchronous Dynamic Random Access Memory
TCP	Time Code Processor