

AXI3910



STANAG3910 TEST & SIMULATION MODULE FOR VXI BUS



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GENERAL FEATURES

The AXI3910 is part of AIM's family of VXibus cards offering full function Test, Simulation, Monitoring and databus analyser functions for STANAG3910 applications. A dual redundant STANAG3910 High Speed and Low Speed interface are available on the C-sized AXI3910 VXI module.

The AXI3910 can be used for Protocol Testing and Simulation of STANAG3910 LS/HS Bus Controller, Multiple Remote Terminals and Chronological Monitoring at full bus load. All operations are performed concurrently with no degradation of performance in any operational mode. The HS section of the AXI3910 supports EFabus Direct Digital Links (DDL).

The AXI3910 incorporates full protocol error injection and detection on both the LS and the HS Bus with software programmable output amplitude and coupling modes of the electrical bus signals. The module fully supports the Protocol Testing requirements defined by the Eurofighter RT and BC Production Test Plans.

The AXI3910 module operates with the optionally provided PBA-3910/ParaView STANAG3910 Databus Analyser Software Packages for Windows 98/NT/2000/XP.

An on-board IRIG-B time code decoder and generator allows users to accurately synchronise single or multiple AXI3910 modules to a common time source.

The use of an Application Support Processor (ASP) executing the Driver Software allows user specific test routines to be processed on-board significantly off-loading the host processor. This new concept allows users to implement application specific system level functionality on a single interface card.

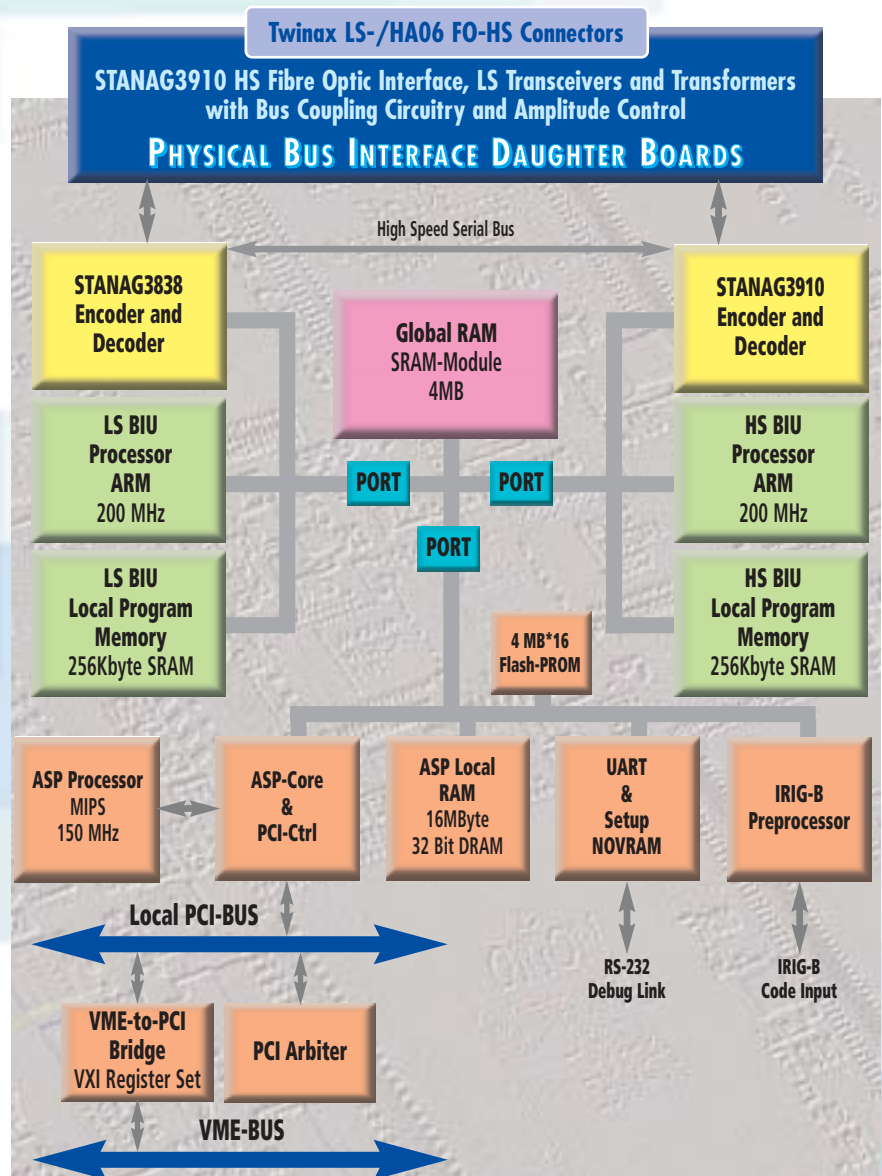
The AXI3910 card uses a 'Common Core' hardware design utilising multiple RISC processors. One of the Physical Bus Interface (PBI) daughter boards provides MIL-STD-1553B Low Speed (LS) bus connections including a resistive terminated bus network. The STANAG3910 High Speed (HS) interface containing a dual redundant Fibre Optic Front End (FOFE) for High Speed (HS) bus operation is included on a second PBI daughter board.

BUS CONTROLLER

The AXI3910 provides real time Bus Controller (BC) functions for one dual redundant STANAG3910 LS/HS databus system concurrently with Multiple LS/HS Remote Terminals (RT's) and LS/HS Chronological Monitor operation. A 200MHz RISC Processor provides true simulation of Bus Controller and multiple Remote Terminal operations without host computer interaction.

The AXI3910 Interface provides multi-buffering and allows the generation of dynamic data functions such as EFabus Dynamic Tags for LS/HS messages.

- ❑ Autonomous operation including sequencing of LS Minor/Major Frames
- ❑ Programmable HS Transmitter Initialise Time & HS Receiver Timeout
- ❑ Full LS/HS Error Injection down to word and bit level
- ❑ Supports EFabus Message Multiplexing
- ❑ External Trigger inputs and output



MULTIPLE REMOTE TERMINAL

The AXI3910 simulates up to 31 LS/HS Remote Terminals with all sub-addresses each providing individually programmable Response Time. Each HS RT simulates all 128 Message Identifiers (MID). LS/HS RT's can be programmed in „Mailbox Monitor Mode“ for non-simulated RT's.

The interface provides multi-buffering, and allows the generation of dynamic data functions such as EFABus Dynamic Tags for LS/HS messages.

- ▣ Programmable RT Response Time down to 4 μ s for each simulated RT
- ▣ Multi-Buffering for each simulated RT, MID and Sub-Address
- ▣ Full LS/HS Error Injection for each simulated RT, Sub-Address and MID down to word and bit level
- ▣ Supports EFABus Message Multiplexing

Multi Level Complex Sequence Trigger on:

- ▣ LS/HS Error, LS/HS Word
- ▣ LS/HS Data Word in Limits

Monitor and Capture:

- ▣ Trigger on Start, Centre and End
- ▣ LS/HS Message and Error Counters
- ▣ LS/HS Data Recording onto Hard Disk

CHRONOLOGICAL BUS MONITOR

The AXI3910 offers powerful LS/HS Bus Monitor functions including comprehensive Bus Monitoring and analysis features with multiple trigger and programmable capture filter capabilities. The Bus Monitor provides accurate Time Tagging of both, LS and HS messages, intermessage gaps, response time and transmitter initialise time. LS/HS messages are time tagged to a 1 μ s resolution. LS Response Time and intermessage gaps as well as HS Transmitter Initialise Time are measured down to 0.25 μ sec.

PHYSICAL BUS REPLAY

The AXI3910 module is able to physically reconstruct previously recorded STANAG3910 databus traffic to the LS/HS databus (electrical and optical) with excellent timing accuracy. Recorded data files can be selected for Physical Bus Replay to perform systems integration and test with the ability to disable any or all RT responses from a recorded file.

IRIG-B TIME CODE DECODER

An on-board IRIG-B time code decoder and generator allows synchronization of AXI3910 modules to a common time source. Multiple AXI3910 modules can be synchronised using one common IRIG-B time source or the on-board time code generator of one AXI3910 module as the reference for accurate correlation of data across multiple STANAG3910 data streams.

APPLICATION SUPPORT PROCESSOR

A 150 MHz ASP Application Support Processor provides unique on-board processing functions typically provided by host processing systems.

- ▣ Driver Software Execution on-board
- ▣ Control of RS232C debug Port for Firmware Updates
- ▣ Dynamic Data Generation
- ▣ Automatic Test Sequence Generation
- ▣ User Application processing on-board

PHYSICAL BUS INTERFACE

A Physical Bus Interface daughter board (PBI) provides STANAG3838 / MIL-STD-1553B transformer or direct bus coupling with variable output transceivers and a resistive bus termination to enable a direct connection of external BC or RT devices. The coupling mode to the external bus system is software programmable.

For HS databus interconnection the AXI3910 module provides a STANAG3910 Physical Bus Interface (PBI) daughter board with on-board dual redundant FOFE.

DRIVER SOFTWARE SUPPORT

With the AXI3910 module a VISA compatible VXI „plug&play“ driver software package is included. Soft Front Panels and Function Panels processed under LabWindows/CVI are also provided.

TECHNICAL DATA

AXI3910 Module

Sub-System Interface:

VMEbus Slave, Options D8, D16, D32, A32 or A24
1 interrupt level used "Interrupt Release on Acknowledge"
Register based VXI device

Processors:

Two 32 Bit StrongARM 200MHz Processors
One 64 Bit MIPS 150MHz Processor

Memory:

4 Mbyte Global RAM
16 Mbyte ASP RAM

Encoder/Decoder:

STANAG3910 / MIL-STD-1553B Encoder/Decoder
with full Error Injection / Detection Capability

Time Tagging:

46 Bit absolute IRIG-B Time Code
1µs resolution

Physical Bus Interface:

Dual Redundant MIL-STD-1553B Transceiver with Variable
Output Amplitude and programmable Bus Coupling with
on-board terminated Bus Network.
Dual redundant STANAG3910 Fibre Optic Front End (FOFE)

FOFE

FO Transmitter:

-0.5 dBm ± 3.5 dB peak Output Power
into 200/280µm fibre @ 810nm wavelength

FO Receiver:

-35 dBm peak Sensitivity @ 10⁻⁹ BERR
-23 dB operating range

Connectors:

Two "HA" Type FO connectors
for HS Bus Interconnection

Connectors:

- 2 x 96 way VMEbus backplane connectors
- 9 way D-Sub Trigger/Time Code connector
- 4 Twinax Connectors (Bus & Stub)
for LS Bus Interconnection

Dimensions:

C-sized VXI Module
340 mm x 233 mm x 30 mm

Power Consumptions

17.5 Watts typical @ 5VDC
2.5 Watts typical @ 12VDC

Operating Temp. Range:

Standard: 0°C ... +45°C ambient
Extended: -15°C ... +60°C ambient

Storage Temp. Range:

-40°C ... +85°C ambient

Humidity:

0 to 95% non-condensing



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ORDERING INFORMATION

AXI3910

Dual Redundant STANAG3910 Tester Module
for the VXIbus: BC, Multi RT, Mailbox and Chronological
Monitor including IRIG-B Time Decoder.
4 Mbyte Global RAM, 16 Mbytes ASP RAM
Dual Redundant Fibre Optic Front End (FOFE)

For EFAbus Express Version use: AXI3910-XP

AXI3910S

Simulator only configuration available

For EFAbus Express Version use: AXI3910S-XP

AXI3910M

Monitor only configuration available

For EFAbus Express Version use: AXI3910M-XP

