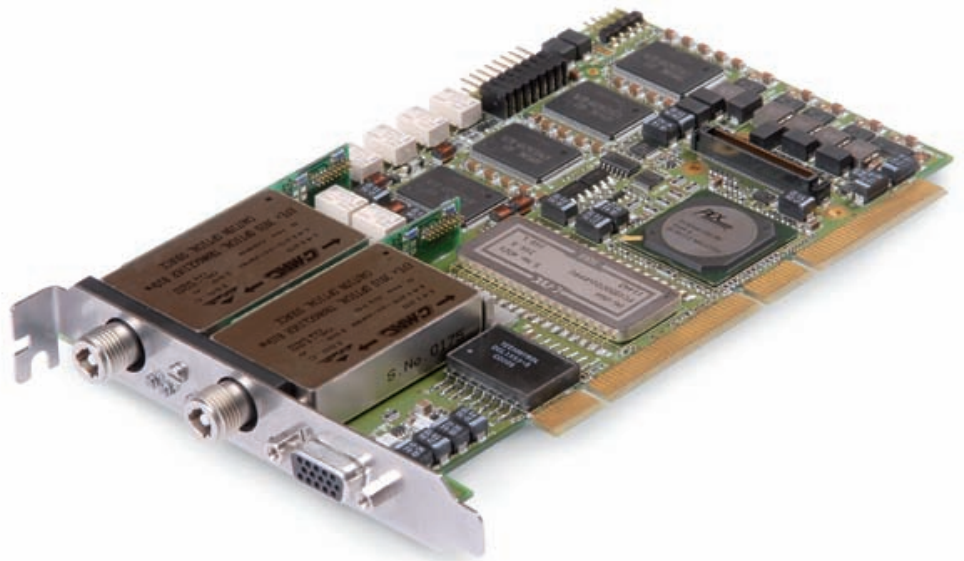


APX3910

STANAG3910/EFEX Test
& Simulation Module
for PCI-X



General Features

The APX3910 is a member of AIM's new 4th generation family of advanced PCI-X modules for analysing, simulating, monitoring and testing of STANAG3910/ EFABus Express (EFEX) databuses. A single stream, dual redundant STANAG3910 High Speed and STANAG3838 Low Speed interface is provided by the APX3910 in a 'Short Length PCI-X' standard module format.

The APX3910 can be used for Protocol Testing and Simulation of STANAG3910 LS / HS Bus Controller, Multiple Remote Terminals and Chronological Monitoring at full bus loads. All BC/RT/BM operations are performed concurrently with no degradation of performance in any operational LS / HS mode. The HS section of the APX3910 supports EFABus Direct Digital Links (DDL) and Fibre Optic DDL (FODDL) acquisition. EFABus Express (EFEX) extensions to the STANAG3910 protocol are fully supported by the Board Software Package (BSP) and a switching key to select between both modes of operation. The APX3910 incorporates full protocol error injection and detection.

The physical STANAG3910 replay function reconstructs and replays previously recorded electrical / optical STANAG3910 bus traffic to the LS/HS databus with excellent timing accuracy. The module supports Protocol Testing requirements defined by the Eurofighter RT and BC Production Test Plans.

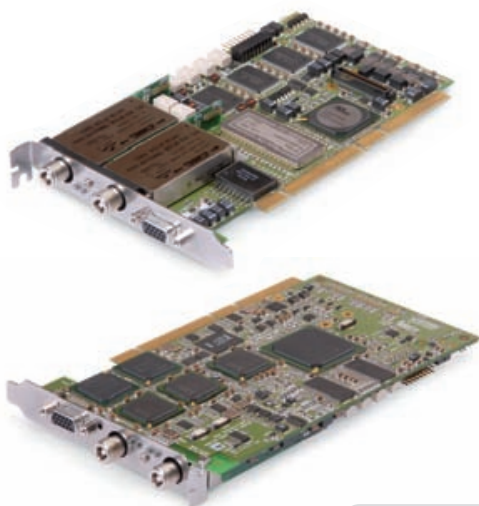
The APX3910 card uses a 'New Common Core' (NCC) design with multiple RISC processors and up to 16MB of global RAM and 64Mbytes of ASP RAM. An Application Support Processor (ASP) executes the Driver Software on board. The ASP provides powerful on board processing and large memory resources, which supports user developed real time applications and minimises host processor interaction.

An on-board IRIG-B time generator/decoder is included for time tag synchronisation at the system level for single or multiple APX3910 modules. The APX3910 Physical Bus Interface (PBI) includes a Fibre Optic Front End and 1553 Transceiver (TRAFO) implemented on a single PCI-X module including both High Speed (HS) and MIL-STD-1553B Low Speed (LS) bus connections. A resistive terminated bus network, Trigger I/O and IRIG-B signals are provided. Optional Bus Analyser Software is available and supports both STANAG3910 and EFEX applications.

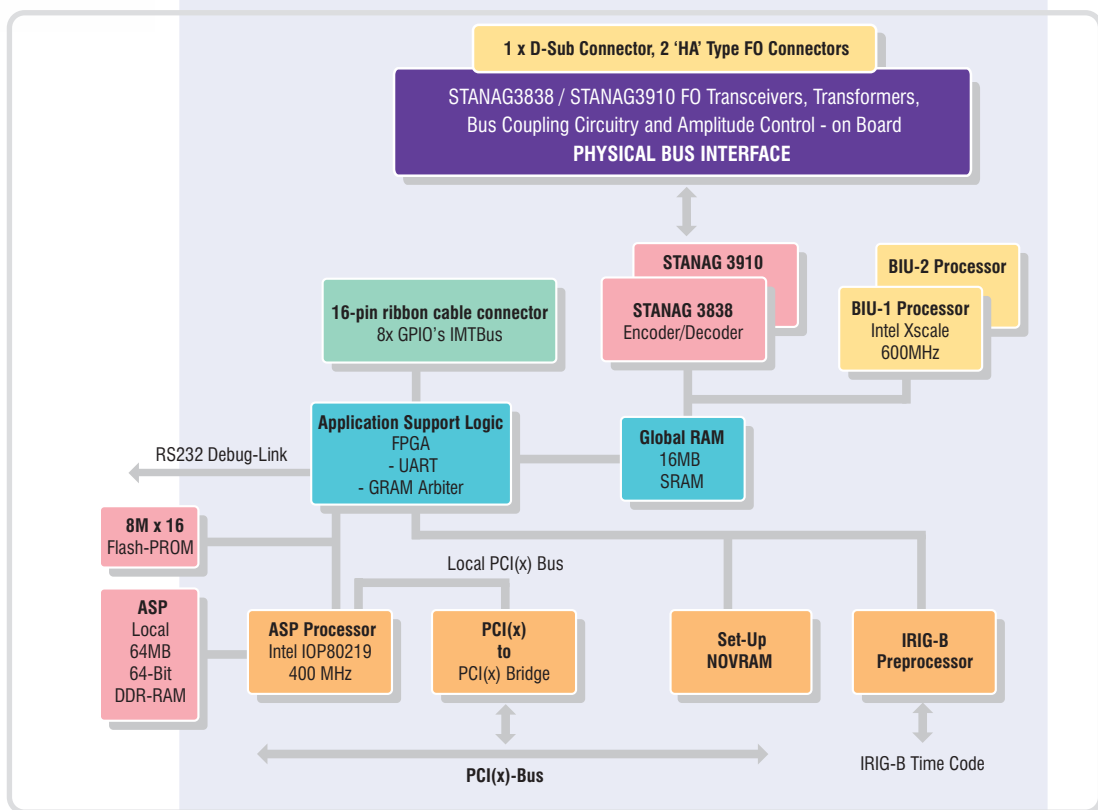
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product guide



APX3910 Functional Block Diagram



Bus Controller

The APX3910 provides a real time Bus Controller (BC) function for one dual redundant STANAG3910 LS/HS databus system including Data buffer queues for generation of dynamic data functions such as EFABus Dynamic Tags for LS/HS messages.

Key Features of the Bus Controller Mode include:

- Autonomous operation including sequencing of LS Minor/Major Frames
- Acyclic message insertion/deletion
- Programmable BC Retry without host interaction
- Programmable HS Transmitter initialise Time & HS Receiver Timeout
- Full LS/HS Error Injection down to word and bit level
- Supports EFABus Message Multiplexing
- Multi-buffering with Real Time Data Buffer Updates
- Synchronisation of BC operation to external trigger inputs
- LS Bus 4usec Intermessage gaps

Multiple Remote Terminal

The APX3910 can simulate up to 31 LS/HS Remote Terminals with all sub-addresses each providing individually programmable Response Time. Each HS RT simulates all 128 Message Identifiers (MID). LS/HS RT's can be programmed in 'Mailbox Monitor Mode' for non-simulated RT's.

The interface provides data buffer queues allowing the generation of dynamic data functions such as EFABus Dynamic Tags for LS/HS messages.

Key features of the Remote Terminal Simulation Mode include:

- Programmable Response Time for Each RT with fast RT Response at 4 μ s.
- Multi-Buffering for each simulated RT, MID and Sub-Address
- Full LS/HS Error Injection for each simulated RT, Sub-Address and MID down to word and bit level
- Programmable & Intelligent Response to Mode Codes
- Multi-Buffering with Real Time Data Buffer Updates
- Supports EFABus Message Multiplexing

Chronological Bus Monitor

The APX3910 includes a powerful LS/HS Bus Monitor and analysis function with multiple trigger and programmable capture capabilities. Accurate Time Tagging of both LS and HS messages, intermessage gaps, response time and transmitter initialise time is supported. LS/HS messages are time tagged to a 1 μ s resolution. LS Response Time and intermessage gaps as well as HS Transmitter Initialise Time are measured down to 0.25 μ s.

Key features of the Chronological Bus Monitor include:

Multi Level Complex Sequence Trigger on:

- LS/HS Error, LS/HS Word
- LS/HS Data Word in Limits

Monitor and Capture

- Up to 16 Mbytes of on-board memory for LS/HS messages
- Trigger on Start, Centre and End
- LS/HS Message Counters

Physical Bus Replay

The APX3910 module can reconstruct previously recorded STANAG3910 databus traffic to the LS/HS databus with excellent timing accuracy. Recorded data files can be selected for Physical Bus Replay to perform systems testing with the ability to disable any or all RT responses from a recorded file.

EFABus Express(EFEX) Functionality

The APX3910 module supports EFABus Express (EFEX) protocol in all operating modes and at full bus rates. EFEX protocol is co-resident with STANAG3910 functionality to support either Tranche I or Tranche II Typhoon Aircraft standards. Selection of STANAG3910 or EFEX mode is via a software 'switch' fully accessible at the API Level or via dedicated bus analyser software.

Key functions of the EFEX mode operation include:

EFEX Bus Control

- EFEX Bus Controller Simulation of all Transfer types
- Control, Status & Status/Data Command Frame Control
- Simulation of Gap and Wait time Setting Control
- EFEX Mode Code support
- Error/Injection Detection
- EFEX Mixed Mode Simulation & Monitoring

EFEX RT Simulation

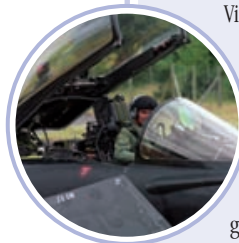
- EFA / EFEX Dual Mode RT Simulation for all EFEX BC Commands
- EFEX HS RT Response Time Setting Control for SD & S Frame
- HS Mode Code Simulation for EFEX RTs
- Error Injection

EFEX Bus Monitoring

- Chronological & Mailbox Bus Monitoring of EFEX Bus Traffic
- Capture & Decoding of CC/MC, SD/S Frames with Time Tag
- Monitor Trigger on Command, SD/S Frame, ADW & DSI
- EFEX Transfer Error Detection
- Monitor Trigger on HS Frame Bus Errors
- EFEX Bus Recording & Replay at full bus rates

EFEX Bus Analyser Software

AIM provides Bus Analyser Software now specially extended to include EFEX data bus testing applications offered as PBA3910, ParaVIEW-3910 Visualiser Software and PBA.pro Databus Analyser Software Packages for Windows 2000/XP.

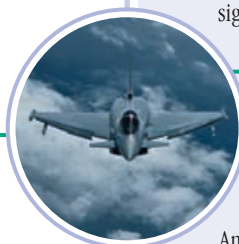


IRIG-B Time Code Decoder

APX3910 modules include an on-board IRIG-B time decoder and generator with a sinusoidal output with a 'free wheeling' mode for time tag synchronisation. This allows synchronisation of multiple APX3910 modules to one common external IRIG-B time input source. Alternatively the on-board time code generator of one APX3910 module in the system can act as a reference for correlation of data captured across multiple STANAG3910/EFEX bus streams.

Physical Bus Interface

The Physical Bus Interface (PBI) including Fibre Optic Front End (FOFE) and 1553 Transceiver (TRAFO) are implemented completely on a single board. Bus Interface Unit (BIU) Processors support the encoder/decoder functions for 3910/EFEX and STANAG3838/MIL-STD-1553A/B protocols. The APX3910 main board also supports both High Speed (HS) and MIL-STD-1553B Low Speed (LS) bus connections including a resistive terminated bus network as well as I/O connections for Triggering and IRIG-B signals. Coupling of an external bus system is software programmable.



Driver Software Support

The Driver Software resides on the APX3910 module instead of the Host Processor for higher performance and efficiency.

An Application Programming Interface (API) is provided compatible with Windows 2000/XP and Linux. Host Applications can be written in MSVC, Visual Basic, Delphi, Borland C++ etc. LabVIEW VIs and a LabWindows/CVI application interface are additionally provided

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Application Support Processor

The onboard Application Support Processor (ASP) offers processing functions typically provided by host processor system.

Operational features include:

- Driver Software Execution on-board
- Dynamic Data Generation
- Customer Specific Programming of the ASP
- Runs under Nucleus + Operating System

Technical Data

Sub-System Interface:

PCI-X Bus Master & Slave, Revision 2.3, 33/66/100/133MHz, 32/64-Bit, 5V & 3.3V compatible.

Processors:

Two 32-Bit 600MHz XScale Processors for 1553 & 3910 BIUs, 32 Bit 400MHz Intel IOP for ASP with 64Bit Data Path.

Memory:

16 Mbyte Global SRAM, 64Mbyte ASP DDR-RAM.

Encoder/Decoder:

STANAG3910 / STANAG3838 Transceiver (TRAFO) with full Error Injection & Detection Capability.

Time Tagging:

46 Bit absolute IRIG-B Time with 1µs resolution, sinusoidal IRIG-B output with 'free wheeling' mode.

Physical Bus Interface (PBI):

Physical Bus Interface (PBI) including Fibre Optic Front End and STANAG3838 Transceiver (TRAFO). Dual Redundant STANAG3838 / MIL-STD-1553B Transceiver with Variable Output Amplitude and Programmable Bus Coupling and on-board terminated Bus Network.

Connectors:

2 HA Aircraft style Fibre Optic Connectors, Normal orientation and STANAG3838 / MIL-STD-1553B connections via High-Density DSUB 15 Way Connector including TTL Trigger, RS-232 Maintenance and IRIG-B Time Code I/O signals. All front plate mounted.

Dimensions: 175mm x 107mm short length PCI format.

Power Consumption: 13.5 Watts typical @ 5V DC Supply.

Operating Temp. Range: Standard 0°C...+45°C. Extended -15°C...+60°C ambient.

Storage Temp. Range: -40°C...+85°C ambient.

Humidity: 0 to 85% non-condensing.

Ordering Information

APX3910

Single Stream, Dual Redundant PCI-X to STANAG3910/EFEX Interface: BC and Multi-RT Simulator with Mailbox & Chronological Monitor. On board Fibre Optic Front End and STANAG3838/MIL-STD-1553A/B Transceiver (TRAFO). IRIG-B Time Encoder / Decoder sinusoidal output. 16MByte Global RAM, 64MByte ASP RAM.

APX3910-S

Single Stream, Dual Redundant PCI-X to STANAG3910/EFEX Interface: BC and Multi-RT Simulator only variant with Mailbox Monitor. On board Fibre Optic Front End and STANAG3838/MIL-STD-1553A/B Transceiver (TRAFO). IRIG-B Time Encoder / Decoder sinusoidal output. 16MByte Global RAM, 64MByte ASP RAM.

APX3910-M

Single Stream, Dual Redundant PCI-X to STANAG3910/EFEX Interface: Monitor only variant with Mailbox & Chronological Monitor with on board Fibre Optic Front End and STANAG3838/MIL-STD-1553A/B Transceiver (TRAFO). IRIG-B Time Encoder / Decoder sinusoidal output. 16MByte Global RAM, 64MByte ASP RAM.

ACB3910-HD15

Ready made Adaptor Cable (2 Metres) from 15 Pin High-Density D-Sub to 2 x Twinax Connectors and 15 Pin standard D-Sub for Trigger, RS-232 Maintenance and IRIG-B Time Code Signals.

